

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> ( Not for submission under 37 CFR 1.99)	Application Number		10002217
	Filing Date		2001-11-01
	First Named Inventor	Craig Nemecek	
	Art Unit	2123	
	Examiner Name	Jason Scott Proctor	
	Attorney Docket Number	CD01207M	

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1	BURSKY, "FPGA Combines Multiple Interfaces and Logic," Electronic Design, Vol. 48 No. 20, pp.74-78 (2 October 2000); 5 pages	<input type="checkbox"/>
2	ANONYMOUS, "Warp Nine Engineering - The IEEE 1284 Experts-F/Port Product Sheet," undated web page found at <a href="http://www.fapo.com/fport.htm">http://www.fapo.com/fport.htm</a> ; 2 pages	<input type="checkbox"/>
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4	Nam et al.; "Fast Development of Source-Level Debugging System Using Hardware Emulation"; IEEE 2000; 4 pages	<input type="checkbox"/>
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7	Oh et al.; "Emulator Environment Based on an FPGA Prototyping Board"; IEEE 21-23; June 2000; 6 pages	<input type="checkbox"/>
8	Hong et al.; "An FPGA-Based Hardware Emulator for Fast Fault Emulation"; IEEE 1997; 4 pages	<input type="checkbox"/>
9	Ching et al.; "An In-Circuit-Emulator for TMS320C25"; IEEE 1994; 6 pages	<input type="checkbox"/>
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11	Melear; "Using Background Modes for Testing, Debugging and Emulation of Microcontrollers"; IEEE 1997; 8 pages	<input type="checkbox"/>

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12	WALTERS, STEPHEN; "Computer-Aided Prototyping for ASIC-Based Systems", 1991, IEEE Design & Test of Computers; Volume 8, Issue 2; 8 pages	<input type="checkbox"/>
13	Anonymous; "JEEN JTAG Embedded Ice Ethernet Interface"; August 1999; Embedded Performance, Inc.; 3 pages	<input type="checkbox"/>
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17	Stallman et al.; "Debugging with the GNU Source-Level Debugger"; January 1994; retrieved on May 2, 2005 from <a href="http://www.cs.utah.edu">http://www.cs.utah.edu</a> ; 4 pages	<input type="checkbox"/>
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23	"In-Circuit Emulators - descriptions of the major ICEs around"; retrieved on November 14, 2005 from <a href="http://www.algonet.se/~staffann/developer/emulator.htm">http://www.algonet.se/~staffann/developer/emulator.htm</a> ; 6 pages	<input type="checkbox"/>
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28	CD00186; "Method for Breaking Execution of a Test Code in DUT and Emulator Chip Essentially Simultaneously and Handling Complex Breakpoint Events;" October 10, 2001; 09/975,338; Nemecek et al.; 34 pages	<input type="checkbox"/>
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33	Bauer et al.; "A Reconfigurable Logic Machine for Fast Event-Driven Simulation"; 1998; Design Automation Conference Proceedings; 8 pages	<input type="checkbox"/>

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	34	Jonathan B. Rosenburg, "How Debuggers Work" John Wiley & Sons, Inc. 1996; 259 pages	<input type="checkbox"/>
	35	USPTO Final Rejection for Application Number 10/001,478 (CD01213M) dated 04/20/2009; 16 pages	<input type="checkbox"/>
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